In the Claims

The following is a copy of Applicant's claims that identifies language being added with underlining ("___") and language being deleted with strikethrough ("—"), as is applicable:

1-7. (Canceled)

8. (Previously presented) An amplifier system, comprising:

a variable gain amplifier having:

a differential pair circuit having a first three terminal device and a second three terminal device;

a first control terminal that receives a first control voltage derived from a differential input control voltage;

degeneration resistive elements coupled between the differential pair circuit and the first control terminal;

a second control terminal that receives a second control voltage derived from the differential input control voltage, the second control voltage opposite in polarity to the first control voltage; and

collector load resistive elements coupled between the differential pair circuit and the second control terminal, the collector load resistive elements being substantially the same type as the degeneration resistive elements, wherein a gain of the system is determined by a physical dimension ratio of the collector load resistive elements to the degeneration resistive elements for the differential input control signal equal to zero volts;

a second variable gain amplifier having:

a second differential pair circuit having a first three terminal device and a second three terminal device;

a third control terminal that receives a third control voltage derived from a second differential input control voltage;

second degeneration resistive elements coupled between the second differential pair circuit and the third control terminal;

a fourth control terminal that receives a fourth control voltage derived from the second differential input control voltage, the fourth control voltage opposite in polarity to the third control voltage; and

second collector load resistive elements coupled between the second differential pair circuit and the fourth control terminal, the second collector load resistive elements being substantially the same type as the second degeneration resistive elements, wherein a gain of the second variable gain amplifier is determined by a physical dimension ratio of the second collector load resistive elements to the second degeneration resistive elements at the second differential input control voltage equal to zero volts, wherein the gain of the second variable gain amplifier is inversely proportional to the gain of the variable gain amplifier.

9. (Original) The system of claim 8, wherein the degeneration resistive elements and the collector load resistive elements include a plurality of three terminal devices.

10. (Original) The system of claim 8, wherein the degeneration resistive elements and the collector load resistive elements include a plurality of resistors.

11. (Original) The system of claim 8, further including a first resistive circuit coupled between the first control terminal and the degeneration resistive elements, the first resistive circuit for turning on and off a three terminal device of the degeneration resistive elements, and further including a second resistive circuit coupled between the second control terminal and the collector load resistive elements, the second resistive circuit for turning on and off a three terminal device of the collector load resistive elements.

12. (Original) The system of claim 8, wherein the degeneration resistive elements and the collector load resistive elements have substantially equal gate to source voltages when the first control voltage equals zero volts and the second control voltage equals zero volts.

13. (Original) The system of claim 8, further including a current mirror circuit coupled between the differential pair circuit and the collector load resistive elements.

14. (Original) The system of claim 13, wherein the current mirror circuit includes at least one of p-channel metal oxide semiconductor (PMOS) transistors and p-type, n-type, p-type material (PNP) transistors, the differential pair circuit includes at least one of n-type, p-type, n-type material (NPN) transistors and n-channel metal oxide semiconductor (NMOS) transistors, and the collector load and the degeneration element include at least one of n-channel metal oxide semiconductor (NMOS) transistors and PMOS transistors.

15. (Original) The system of claim 13, wherein the current mirror circuit includes at least one of NMOS transistors and NPN transistors, the differential pair circuit includes at least one of p-type, n-type, p-type material (PNP) transistors and PMOS transistors, and the

collector load and the degeneration element include at least one of PMOS transistors and NMOS transistors.

16. (Original) The system of claim 8, wherein the variable gain amplifier operates in at least one of a baseband frequency, and an intermediate frequency, and a radio frequency.

17. (Canceled)

18. (Canceled)

19. (Previously presented) The system of claim 8, wherein the second variable gain amplifier is operated at a second frequency and the variable gain amplifier is operated at a first frequency.

20. (Previously presented) The system of claim 8, wherein the second variable gain amplifier is in a feedback loop of the variable gain amplifier.

21. (Previously presented) The system of claim 8, wherein the second variable gain amplifier operated at a first frequency is cascaded to the variable gain amplifier operated at the first frequency.

22. (Previously presented) The system of claim 8, wherein the second degeneration resistive elements and the second collector load resistive elements includes at least one of a three terminal device and a resistor.

23. (Previously presented) A method of operating a variable gain amplifier, comprising:

providing an input signal to a differential pair circuit;

loading the differential pair circuit with degeneration resistive elements and collector load resistive elements;

applying a first control voltage to the degeneration resistive elements;

applying a second control voltage to the collector load resistive elements that is opposite in polarity to the first control voltage;

configuring the degeneration resistive elements to be substantially the same type as the collector load resistive elements, wherein a gain of the variable gain amplifier is determined by a physical dimension ratio of the collector load resistive elements to the degeneration resistive elements at a differential input control voltage equal to zero volts;

providing, loading, applying, and configuring for a second variable gain amplifier;

operating the variable gain amplifier at a first frequency and the second variable gain amplifier at a second frequency; and

effecting a gain of the second variable gain amplifier to be inversely proportional to the gain of the variable gain amplifier.

24. (Original) The method of claim 23, further including turning on and off three terminal devices of the degeneration resistive elements element and the collector load resistive elements.

25. (Original) The method of claim 23, further including mirroring the current of the differential pair circuit to the collector load resistive elements.

26. (Canceled)

27. (Canceled)

28. (Canceled)

29. (Previously presented) The method of claim 23, further including positioning the second variable gain amplifier in a feedback loop of the variable gain amplifier.

30. (Previously presented) The method of claim 23, further including cascading the second variable gain amplifier at a first frequency to the variable gain amplifier operated at the first frequency.

31. (Previously presented) The method of claim 23, further including deriving the first control voltage and the second control voltage from the differential input control voltage.

32. (Original) An amplifier system, comprising:

a first variable gain amplifier having:

a first differential pair circuit having a first three terminal device and a second three terminal device, the first and the second three terminal devices each having an emitter terminal, a collector terminal, and a base terminal;

a first control terminal that receives a first control voltage;

a variable emitter load coupled to the emitter terminals of the first differential pair circuit;

a constant resistance load coupled to the collector terminals of the first differential pair circuit; and

a second variable gain amplifier having:

a second differential pair circuit having a first three terminal device and a second three terminal device, the first and the second three terminal devices each having an emitter terminal, a collector terminal, and a base terminal;

a second control terminal that receives a second control voltage;

a variable collector load coupled to the collector terminals of the first differential pair circuit; and

a second constant resistance load coupled to the emitter terminals of the first differential pair circuit, wherein the variable emitter load is of substantially the same type as the variable collector load, wherein a gain of the variable gain amplifier system is dependent on a physical size ratio of the variable collector load to the variable emitter load at a differential input control voltage equal to zero volts.

33. (Original) The system of claim 32, wherein the first variable gain amplifier operates at a first frequency and the second variable gain amplifier operates at a second frequency.

34. (Original) The system of claim 32, further including a plurality of at least one of the first variable gain amplifier and the second variable gain amplifier.

35. (Original) The system of claim 32, wherein a gain of the first variable gain amplifier is inversely proportional to a gain of the second variable gain amplifier.

36. (Original) The system of claim 32, wherein the variable collector load and the variable emitter load includes NMOS transistors.

37. (Original) The system of claim 32, wherein the variable collector load and the variable emitter load includes PMOS transistors.

38. (Original) The system of claim 32, further including current mirror circuits that mirror current of the second differential pair circuit to the variable collector load.

39. (Original) The system of claim 32, wherein the first control voltage increases proportionally to the second control voltage and the first control voltage decreases proportionally to the second control voltage.

40. (Currently amended) The system of claim 32, wherein the gain is dependent on a physical size ratio of the variable collector load to the variable emitter load when the first control voltage and the second control voltage ~~equals~~ are equal, wherein the first control voltage and the second control voltage are derived from the differential input control voltage.

41. (Original) A method of operating a variable gain amplifier system, comprising:

providing a first input signal to a first differential pair circuit and a second differential pair circuit, the first differential pair circuit and the second differential pair circuit including emitter terminals, base terminals, and collector terminals;

loading the emitter terminals of the first differential pair circuit with a variable emitter load;

loading the collector terminals of the first differential pair circuit with a constant resistance load;

controlling the variable emitter load with a first control voltage;

loading the emitter terminals of the second differential pair circuit with a constant resistance load;

loading the collector terminals of the second differential pair circuit with a variable collector load; and

configuring the variable collector load to be substantially the same type as the variable emitter load, wherein a gain of the variable gain amplifier system is dependent on a physical size ratio of the variable collector load to the variable emitter load at a differential input control voltage equal to zero volts.

42. (Original) The method of claim 41, further including mirroring current of the second differential pair circuit to the variable collector load.

43. (Original) The method of claim 41, further including increasing the first control voltage while proportionally increasing the second control voltage.

44. (Original) The method of claim 41, further including decreasing the first control voltage while proportionally decreasing the second control voltage.

45. (Previously presented) A transceiver, comprising:

an amplifier system, comprising:

a first variable gain amplifier having:

a first differential pair circuit having a first three terminal device and a second three terminal device, the first and the second three terminal devices each having an emitter terminal, a collector terminal, and a base terminal;

a first control terminal that receives a first control voltage;

a variable emitter load coupled to the emitter terminals of the first differential pair circuit;

a constant resistance load coupled to the collector terminals of the first differential pair circuit; and

a second variable gain amplifier having:

a second differential pair circuit having a first three terminal device and a second three terminal device, the first and the second three terminal devices each having an emitter terminal, a collector terminal, and a base terminal;

a second control terminal that receives a second control voltage;

a variable collector load coupled to the collector terminals of the first differential pair circuit; and

a second constant resistance load coupled to the emitter terminals of the first differential pair circuit, wherein the variable emitter load is of substantially the same type as the variable collector load, wherein a gain of the variable gain amplifier system is dependent on a physical size ratio of the variable collector load to the variable emitter load at a differential input control voltage equal to zero volts.

46. (Previously presented) The transceiver of claim 45, wherein the first variable gain amplifier operates at a first frequency and the second variable gain amplifier operates at a second frequency.

47. (Previously presented) The transceiver of claim 45, further including a plurality of at least one of the first variable gain amplifier and the second variable gain amplifier.

48. (Previously presented) The transceiver of claim 45, wherein a gain of the first variable gain amplifier is inversely proportional to a gain of the second variable gain amplifier.

49. (Previously presented) The transceiver of claim 45, wherein the variable collector load and the variable emitter load includes NMOS transistors.

50. (Previously presented) The transceiver of claim 45, wherein the variable collector load and the variable emitter load includes PMOS transistors.

51. (Previously presented) The transceiver of claim 45, further including current mirror circuits that mirror current of the second differential pair circuit to the variable collector load.

52. (Previously presented) The transceiver of claim 45, wherein the first control voltage increases proportionally to the second control voltage and the first control voltage decreases proportionally to the second control voltage.

53. (Currently amended) The transceiver of claim 45, wherein the gain is dependent on a physical size ratio of the variable collector load to the variable emitter load when the first control voltage and the second control voltage ~~equals~~ are equal, wherein the first control voltage and the second control voltage are derived from the differential input control voltage.

54. (Previously presented) The transceiver of claim 45, wherein the amplifier system is incorporated in a polar loop system.